

ABSTRACT

APPARATUS FOR TESTING COMPUTER MEMORY

5 An electronic memory device tester has an input
arranged to receive seed data with a first number (p)
of seed data bits from a computer and a data generator
arranged to receive an array of prepared data having a
second number (q) of prepared data bits, where $q > p$, and
10 arrange to generate from the prepared data a test data
pattern for writing to an electronic memory device to
be tested. The tester generates its own test pattern
thus relieving the computer processor from that task.
This in turn allows the computer to control the test
15 cycle itself without compromising the test speed.

Figure 1 for Abstract

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